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EXAMINER	
CHAUDRY, MUJTABA M	

ART UNIT	PAPER NUMBER
2133	4

DATE MAILED: 04/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/835,170	Applicant(s) GOLD, SPENCER	
	Examiner Mujtaba K Chaudry	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6 and 24-29* is/are pending in the application.

4a) Of the above claim(s) *7-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 24-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-29* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *06 August 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *4*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

A provisional restriction requirement was made on Thursday, March 18, 2004 with Applicant's Attorney, David Burns (617-227-7400). See interview summary attached. Examiner hereby makes acknowledgement of Applicant's oral election without traverse of Group I, which include claims 1-6 and 24-29 and are classified in class 714/738.

Applicant is also reminded that affirmation for the elected group and cancellation of nonelected claims of Group II, which include claims 7-14, classified in class 714/720, and Group III, which include claims 15-23, classified in 714/733, must be made in subsequent communication.

Claims of Group I, consisting of claims 1-6 and 24-29 are herein considered for examination. Claims 7-23 are withdrawn from consideration. (37 CFR 1.144) See MPEP § 821.01. As for the record, the following is a formal restriction with regards to Groups I, II and III.

Restrictions to one of the following inventions is required under 35 USC 121:

I. Claims 1-6 and 24-29, drawn to an integrated circuit comprising a memory array coupled test generator and a conversion circuit, classified in class 714, subclass 738.

II. Claims 7-14, drawn to an method for testing an integrated circuit with a test vector for a first address and determining a second address based on the first address, classified in class 714, subclass 720.

III. Claims 15-23, drawn to a method for performing built-in self-testing on memory array, classified in class 714, subclass 733.

The inventions are distinct, each from the other because of the following reasons:

Inventions Group I, an integrated circuit comprising a memory array coupled test generator and a conversion circuit and Group II, an method for testing an integrated circuit with a test vector for a first address and determining a second address based on the first address are related as combination and subcombination. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the claims of Group I do not require the limitations of providing a first test vector for a first address memory and in particular, determining a second address of the memory based on the first address. The subcombination has separate utility such as in a single networked environment.

Inventions Group I, an integrated circuit comprising a memory array coupled test generator and a conversion circuit and Group III, a method for performing built-in self-testing on memory array. Inventions in this relationship are distinct if it can be shown that (1) the combination as claimed does not require the particulars of the subcombination as claimed for patentability, and (2) that the subcombination has utility by itself or in other combinations (MPEP § 806.05(c)). In the instant case, the combination as claimed does not require the particulars of the subcombination as claimed because the claims of Group I do not require the

limitations of a method for performing built-in self-testing. The subcombination has separate utility such as in a single networked environment.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group II, restriction for examination purposes as indicated is proper.

Because these inventions are distinct for the reasons given above and the search required for Group I is not required for Group III, restriction for examination purposes as indicated is proper.

Drawings

The drawings are objected to because:

- In Figure 1, reference 23 should be labeled as "data transmission path" as indicated in the specification, page 8, lines 3-4.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 24 recites the limitation "the test vector circuit" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim. For examination purposes, the Examiner will assume "test vector circuit" and "test circuit" to be of the same.

Dependent claims 25-29 inherently include limitations from independent claim 24 and therefore are rejected as well. Applicants are recommend to modify claim language so that it is uniform.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 24 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamada et al.

As per claims 1 and 24, Yamada et al. (herein after: Yamada) teaches (title, abstract and Figure 1) a method and apparatus for generating patterns for SDRAM memory. A test pattern is generated for the SDRAM by having a specific wrap conversion circuit or an address conversion method. The wrap conversion circuit is provided to receive two kinds of data from a pattern generator and converts the data through a predetermined logic circuit information. The test pattern generation method for the SDRAM is carried out by inputting the column address data Y0-Y2 and the wrap address data Z0-Z2, and by generating output data which has been converted by a predetermined logic equation. The test pattern generation apparatus and method can also include an address inversion scramble for the converted output. Furthermore, Yamada teaches (Figure 1) the wrap address conversion circuit 40 is provided at an output of a pattern

generator 10. For the wrap address conversion circuit 40, data (Y0-Y8) corresponding to the bit length of the column address of the SDRAM is provided from the pattern generator 10. At the same time, data (Z0-Z2) corresponding to the bit length of the wrap address of the SDRAM is provided to the wrap address conversion circuit 40 from the pattern generator 10. Yamada also teaches (col. 4, lines 25-65) the address inversion scramble is used for converting the address between the logical address and the physical address of the device under test. This is a function to convert the address because the chip alignment within the device to be tested is freely designed and determined to meet the physical and operational conditions of the device for each kind of devices and such an alignment does not match the logical address given at the outside of the device. Thus, the address inversion scramble is a function necessary to perform failure analysis with respect to the internal operation of the device under test.

Claim Rejections - 35 USC § 103

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 2-6 and 25-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamada et al. (USPN 5854801).

As per claims 2-4 and 25-27, Yamada et al. (herein after: Yamada) substantially teaches, in view of above rejections, a conversion circuit as shown in Figure 1.

Yamada does not explicitly teach the conversion circuit to comprise of a ROM, RAM or EEPROM as stated in the present application.

However, Yamada teaches (col. 2, lines 10-63) a test pattern generation apparatus is provided to effectively test an SDRAM. The pattern generation apparatus includes a-wrap address conversion means which is provided with two (2) kinds of data (Y0-Y2) and (Z0-Z2) from a pattern generator and outputs converted addresses which have been **converted based on a predetermined logic circuit** information in the conversion means. The Examiner would like to point out that the conversion circuit inherently has to have temporarily storage device, for example a RAM, which is a type of storage memory that can be used while operating. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a RAM, ROM or EEPROM within the conversion circuit of Yamada. This modification would have been obvious to one of ordinary skill because one of ordinary skill would have recognized that the use of EEPROM, RAM or ROM allows the electronic device to detect nonfunctional memory cell locations.

As per claims 5-6 and 28-29, Yamada et al. (herein after: Yamada) substantially teaches, in view of above rejections, the address inversion scramble is used for converting the address between the logical address and the physical address of the device under test. This is a function to convert the address because the chip alignment within the device to be tested is freely designed and determined to meet the physical and operational conditions of the device for each kind of devices and such an alignment does not match the logical address given at the outside of

the device. Thus, the address inversion scramble is a function necessary to perform failure analysis with respect to the internal operation of the device under test. Further, the output of the wrap conversion circuit 40 can be given to a failure analysis apparatus (not shown).

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Yamada teaches a method and apparatus for generating patterns for SDRAM memory. Applicant is invited to read/review additional pertinent prior art that has been included herein.

Any inquiries concerning this communication should be directed to the examiner, Mujtaba Chaudry who may be reached at 703-305-7755. The examiner may normally be reached Mon – Thur 7:30 am to 4:30 pm and every other Fri 8:00 am to 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, please contact the examiner's supervisor, Albert DeCady at 703-305-9595. The fax phone number for the organization where this application is assigned is 703-746-7239.

Any inquiry of general nature or relating to the status of this application or proceeding should be directed to the receptionist at 703-305-3900.

Mujtaba Chaudry
Art Unit 2133
April 22, 2004

Guy J. Lamare
for
Albert DeCady
Primary Examiner